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### REMARKS

Claims 1, 3, 4, 6, 20-26, 30, and 31 are pending in the above-identified application. Claims 1, 4, 20, 21, and 23 have been amended, claim 3 has been canceled, and claim 32 has been added herein. Upon entry of this amendment, claims 1, 4, 6, 20-26, 30, 31, and 32 will be pending in the above-identified application.

Enclosed is a Credit Card Payment Form authorizing payment of the fees for a two month extension of time.

### Claim Objections

Claim 20 has been amended to recite "a first base layer". Additionally, claim 20 recites "a second base layer". Accordingly, Applicant respectfully submits claim 20 has antecedent basis for the recitations of "the first base layer" and "the second base layer" referred to in the Office Action dated April 30, 2003. Therefore, Applicant respectfully requests the objection to claim 20 be withdrawn.

### Section 103

Applicant respectfully requests reconsideration of the rejection of Claims 1, 3, 4, 6, 21-23, 25-26, 30, and 31 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,258,379 (Watanabe) in view of U.S. Patent No. 5,151,765 (Yamauchi) or U.S. Patent No. 4,826,780 (Takemoto).

Claims 1, 4, 6, 21-23, 25, 30, and 31 recite, among other things, a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor each having an emitter. The semiconductor device comprises, among other things, a first embedded diffusion layer and a second embedded diffusion layer, wherein a top of the second embedded diffusion layer is formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between a top of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, and a bottom of the second embedded diffusion layer is formed at a distance from the surface of the emitter of the second vertical type bipolar transistor

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greater than a distance between a bottom of the first embedded diffusion layer and the surface of the emitter of the first vertical type bipolar transistor.

Watanabe discloses a first buried layer 21 and a second buried layer 22", wherein the first buried layer has a top formed at a distance from a surface of an emitter 62 greater than a distance between a top of the second buried layer and the surface of the emitter, and the second buried layer has a bottom formed at a distance from the surface of the emitter greater than a distance between a bottom of the first buried layer. Watanabe discloses the bottom of the second buried layer is formed at a distance from the emitter greater than a distance between the bottom of the first buried layer and the emitter. However, in contrast to the claims Watanabe discloses the top of the second buried layer is formed at a distance from the emitter less than the distance between the top of the first buried layer and the emitter. Accordingly, Watanabe fails to disclose or suggest the features of claims 1, 3, 4, 6, 21-23, 25, 30, and 31 recited above. The secondary references also fail to disclose or suggest these recited features. Accordingly, the Section 103 rejection is improper and should be withdrawn.

Applicant respectfully requests reconsideration of the rejection of claims 1, 3, 4, 6, 20-26, 30, and 31 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,379,726 (Kumamaru) in view of Yamauchi or Takemoto).

Claims 1, 4, 6, 20-26, 30, and 31 recite, among other things, a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor each having an emitter. The semiconductor device comprises, among other things, a first embedded diffusion layer and a second embedded diffusion layer, wherein a top of the second embedded diffusion layer is formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between a top of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, and a bottom of the second embedded diffusion layer is formed at a distance from the surface of the emitter of the second vertical type bipolar transistor greater than a distance between a bottom of the first embedded diffusion layer and the surface of the emitter of the first vertical type bipolar transistor.

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Kumamaru discloses a high breakdown voltage element region 13 having an emitter 19, and a buried layer 14 formed in an epitaxial layer 5 and an epitaxial layer 11. Kumamaru does not disclose or suggest a first embedded diffusion layer and a second embedded diffusion layer, wherein a top of the second embedded diffusion layer is formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between a top of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, and a bottom of the second embedded diffusion layer is formed at a distance from the surface of the emitter of the second vertical type bipolar transistor greater than a distance between a bottom of the first embedded diffusion layer and the surface of the emitter of the first vertical type bipolar transistor. The secondary references also fail to disclose or suggest these recited features. Accordingly, the Section 103 rejection is improper and should be withdrawn.

Applicant respectfully requests reconsideration of the rejection of claim 1 under 35 U.S.C. 103(a) as being unpatentable over Yamauchi or Takemoto.

Claim 1 recites, among other things, a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor each having an emitter. The semiconductor device comprises, among other things, a first embedded diffusion layer and a second embedded diffusion layer, wherein a top of the second embedded diffusion layer is formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between a top of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, and a bottom of the second embedded diffusion layer is formed at a distance from the surface of the emitter of the second vertical type bipolar transistor greater than a distance between a bottom of the first embedded diffusion layer and the surface of the emitter of the first vertical type bipolar transistor.

As discussed above, both Yamauchi and Takemoto, considered alone or in combination, fail to disclose or suggest these recitations of claim 1. Accordingly, the Section 103 rejection of claim 1 is improper and should be withdrawn.

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Applicant respectfully requests reconsideration of the rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Yamauchi in view of Kumamaru.

Claim 24 depends from independent claim 1. As discussed above, both Yamauchi and Kumamaru, considered alone or in combination, fail to disclose or suggest all the recitations of claim 1. Accordingly, the Section 103 rejection of claim 24 is improper and should be withdrawn.

Applicant respectfully requests reconsideration of the rejection of claims 20 and 24 under 35 U.S.C. 103(a) as being unpatentable over Takemoto in view of Kumamaru.

Claims 20 and 24 each depend from independent claim 1. As discussed above, both Takemoto and Kumamaru, considered alone or in combination, fail to disclose or suggest all the recitations of claim 1. Accordingly, the Section 103 rejection of claims 20 and 24 is improper and should be withdrawn.

#### New Claim 32

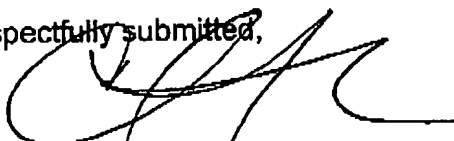
Applicant respectfully submits that none of the cited references, considered alone or in combination, disclose or suggest all the recitations of claim 32. Accordingly, Applicant submits claim 32 is patentable over the cited references.

#### Conclusion

If the Examiner believes that there is any issue which could be resolved by a telephone or personal interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

As it is believed that the application is in condition for allowance, Applicant respectfully requests a favorable action and Notice of Allowance.

Respectfully submitted,



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